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GOLDEN, JAMES R	
ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,510	CHEN ET AL.	
	Examiner	Art Unit	
	James Golden	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application 10/685510 has a total of 12 claims pending. There are 3 independent claims and 9 dependent claims.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference characters not mentioned in the description: I of Figs. 2A, 2B, 4A, 4B, 7A, 7B and 7D; II of Figs. 2C, 4B, 4C, 7B, 7C and 7D; III of Figs. 4C, 7C and 7D. These are presumably the "first batch of data" etc. as referred to on page 3, lines 14-23 and elsewhere in the specification.

3. The drawings are objected to because "First Tier of Data Cache" and "Second Tier of Data Cache" of Fig. 5 are labeled 110 and 112 respectively, but referred to as 124 and 126 in the specification.

4. The drawings are objected to because data packet I of Figs. 7A-7D is not shown in Fig. 7C, but is shown in 7A, 7B and 7D.

5. Figs. 1, 2A, 2B and 2C should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

6. Amendment to the specification to add and correct the reference characters in the description in compliance with 37 CFR 1.121(b) and corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office Action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

7. Applicant is reminded of the proper language and format for an abstract of the disclosure. The form and legal phraseology often used in patent claims, such as "means" and "said," should be removed.

8. The disclosure is objected to because of the following informalities: "become popular" (page 2, lines 8-10) should be corrected to read --are popular-- or --are becoming popular;-- "retrieves" (page 2, line 24) should be corrected to read --retrieve;-- other spelling and grammatical errors were noted, but will not be detailed here. The examiner respectfully requests that the applicant review the specification and make appropriate corrections.

Claim Objections

9. Claim 1 is objected to because of the following informalities: "a" in line 8 and "are" of line 10 are unnecessary and should be removed.

10. Claim 3 is objected to because of the following informalities: "transfer to" should be corrected to --transfer it to.--

11. Claim 5 is objected to because of the following informalities: "the second data caches" should most likely be corrected to --the second data cache.-- It should be noted that the limitation "the second data cache" in line 2 does not imply a first data cache, because it is only dependent on claim 2.

12. Claim 11 is objected to because of the following informalities: "said the storage capacity" should be corrected to --the storage capacity;-- if it were corrected to --said storage capacity,-- it would be rejected under 35 USC § 112, second paragraph.

Double Patenting

13. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA

1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

14. Claims 2-6 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2 and 6-8 of copending Application No. 10/685499.

Instant Application	**Application No. 10/685499**
2. A storage device **capable of increasing transmission speed,**	1. A storage device **available for increasing storage capacity,**
mainly comprising a controller and at least a solid-state storage medium;	comprising a controller and at least a solid-state storage medium;
said controller has an internal system interface that may be connected to an external system end,	said controller having a system interface connected to external system end,

a microprocessor that processes system instructions;	a microprocessor processing system instructions,
and a memory interface that communicates with said solid-state storage medium; wherein	and a memory interface communicating with said solid-state storage medium; wherein:
said storage device is featured with: **a data compression/decompression module with a data compression mechanism**	said controller has **a data compression module**
is devised in said storage device and	**between said system interface and said memory interface, and**
is designed to compress the raw data transferred via the system interface at an **appropriate compression ratio** into compressed data,	the data compression module compresses the original data transferred from the system interface in **1/N compression ratio** under the control of the microprocessor and then
in order to increase data access speed.	**stores the compressed data into said**

	solid-state storage medium via said memory interface.
3. The storage device **capable of increasing transmission speed** as in claim 2, wherein said data compression/decompression module has **an internal decompression mechanism,** which is triggered by the microprocessor to decompress the compressed data stored in said solid-state storage medium into original raw data and transfer it to the system end.	2. A storage device **available for increasing storage capacity** according to claim 1 wherein said storage device has **a data decompression module between said system interface and said memory interface;** said decompression module, under the control of said microprocessor, retrieves compressed data stored in said solid-state storage medium and decompresses it to original data to output.
4. The storage device **capable of increasing transmission speed** as in claim 2, wherein said storage device has the first data	6. A storage device **available for increasing storage capacity** according to claim 2, wherein said storage device has a first data cache

cache, which is wired to said system interface, microprocessor, and data compression/decompression module.	electrically connected to said system interface, said microprocessor, said data compression module and said data decompression module.
5. The storage device **capable of increasing transmission speed** as in claim 2 wherein said controller has the second data caches, which is wired to said memory interface, microprocessor and data compression/decompression module.	7. A storage device **available for increasing storage capacity** according to claim 2, wherein said controller has a second data cache electrically connected to said memory interface, said microprocessor, said data compression module and said data decompression module.
6. The storage device **capable of increasing transmission speed** as in claim 2, wherein said data compression/ decompression module is embedded in said controller and **between said system interface and said memory interface.**	8. A storage device **available for increasing storage capacity** according to claim 2, wherein said data compression module and said data decompression module are **in said controller.**

15. Although the conflicting claims are not identical, they are not patentably distinct from each other.

16. **Claims 2 and 3** of the instant application conflict with claim 2 of Application No. 10/685449.

- The instant application claims "a storage device capable of increasing transmission speed." This is not a limitation but an inherent effect of the claimed invention, as noted by applicant in Application No. 10/685449 (page 8, lines 3-5). Application No. 10/685449 claims "a storage device available for increasing storage capacity," which is also an inherent effect of the claimed invention. These effects are unpatentable and therefore cannot be used to differentiate the claims.
- Claim 1 of Application No. 10/685449 does not explicitly claim a decompression module, but claim 2 does; for this reason, claim 1 of Application No. 10/685449 does not conflict with the instant application.
- Claim 2 of the instant application implies a combined compression and decompression module, while Application No. 10/685449 allows these modules to be combined or separate. Application No. 10/685449 states that "any embodiment implemented with equivalent modifications...(e.g., separate said data compression module and said data decompression module from the controller) shall fall in the scope of the invention" (page 8, lines 17-21), so this is not a patentably distinct difference.

- A "compression module" inherently contains a "compression mechanism," so this mechanism is present in claim 2 of the instant application and claim 1 of Application No. 10/685449.
- The instant application claims the compression/decompression module is "in said storage device" and Application No. 10/685449 claims the compression module is "between said system interface and said memory interface." The wiring scheme required to connect these components effectively makes "in" and "between" equivalent.
- Application No. 10/685449 claims the data is compressed in a "1/N compression ratio." The instant application claims the data is compressed "at an appropriate compression ratio," which is which is defined in the specification as "1/N, wherein 'N' depends on the compression algorithm used..." (page 8, lines 21-22).
- Application No. 10/685449 claims the device "stores the compressed data into said solid-state storage medium via said memory interface." The instant application does not explicitly claim this, but it is a "storage device" and has a solid-state storage medium, so the compressed data must be stored there.
- A "decompression module" inherently contains a "decompression mechanism," so this mechanism is present in claim 3 of the instant application and claim 2 of Application No. 10/685449.

17. **Claim 4** of the instant application directly conflicts with claim 6 of Application No. 10/685449.

18. **Claim 5** of the instant application directly conflicts with claim 7 of Application No. 10/685449.

19. **Claim 6** of the instant application conflicts with claim 8 of Application No. 10/685449.

- As noted above in paragraph 16, "in" and "between have equivalent meanings because of the wiring scheme required to connect these components effectively.

20. Therefore, it would be obvious to a person of ordinary skill in the art that claims 2-6 in the instant application and claims 2 and 6-8 in Application No. 10/685449 claim the same structure differentiated only by unpatentable inherent effects.

21. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 112

22. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

23. **Claims 4 and 5** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

24. **Claim 4** recites the limitation "the first data cache" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim. This rejection could be overcome by correcting this phrase to read --a first data cache.--

25. **Claim 5** recites the limitation "the second data cache" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim. This rejection could be overcome by correcting this phrase to read --a second data cache.--

Claim Rejections - 35 USC § 102

26. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

27. **Claims 1-6** are rejected under 35 U.S.C. 102(b) as being anticipated by Pattisam et al. (US 5,357,614).

28. **With respect to claim 1**, Pattisam et al. disclose a storage device (20 of Fig. 3) capable of increasing transmission speed (inherent effect of compressed data controller of Pattisam et al.), comprising

- a controller (20 of Fig. 3) and
- at least a solid-state storage medium (240 of Fig. 3);
- said controller has an internal system interface that may be connected to
    - an external system end (communications lines 205 and 206 of Fig. 3),
    - a microprocessor that processes system instructions (230 of Fig. 3),
    - and a memory interface that communicates with said solid-state storage medium (215 of Fig. 3);
- wherein said storage device is featured with:

- a plurality of data caches is devised between said system interface and said memory interface (210, 211 and 250 of Fig. 3);

- said data caches are designed in tiers, wherein the first tier of data cache (210 of Fig. 3) and the second tier of data cache (211 of Fig. 3)
  - perform data receiving and transfer alternatively to implement parallel data transmission between said system interface and said memory interface (column 11, lines 65-69 – column 12, lines 1-17).

29. **With respect to claim 2**, Pattisam et al. disclose a storage device (20 of Fig. 3) capable of increasing transmission speed (inherent effect of compressed data controller of Pattisam et al.), mainly comprising

- a controller (20 of Fig. 3) and
- at least a solid-state storage medium (240 of Fig. 3);
- said controller has an internal system interface that may be connected to
  - an external system end (communications lines 205 and 206 of Fig. 3),
  - a microprocessor that processes system instructions (230 of Fig. 3), and
  - a memory interface that communicates with said solid-state storage medium (215 of Fig. 3);
- wherein said storage device is featured with:
  - a data compression/decompression module (222 of Fig. 3; decompression function detailed in column 17, lines 26-31) with
  - a data compression mechanism is devised in said storage device and is designed to compress the raw data transferred via the system interface at

an appropriate compression ratio into compressed data (column 12, lines 33-35),

- in order to increase data access speed (inherent effect of a compression controller).

30. **With respect to claim 3**, Pattisam et al. disclose

- the storage device capable of increasing transmission speed as in claim 2 (see above paragraph 29),
- wherein said data compression/decompression module has an internal decompression mechanism (column 17, lines 26-31), which is triggered by the microprocessor to decompress the compressed data stored in said solid-state storage medium into original raw data and transfer to the system end (column 17, lines 26-31).

31. **With respect to claim 4**, Pattisam et al. disclose

- the storage device capable of increasing transmission speed as in claim 2 (see above paragraph 29),
- wherein said storage device has the first data cache (210 of Fig. 3), which is wired to
  - said system interface (206 of Fig. 3),
  - microprocessor (indirectly through 211 and 216 of Fig. 3), and
  - data compression/decompression module (212 of Fig. 3).

32. **With respect to claim 5**, Pattisam et al. disclose

- the storage device capable of increasing transmission speed as in claim 2 (see above paragraph 29)
- wherein said controller has the second data cache (211 of Fig. 3), which is wired to
    - said memory interface (connection between 211 and 215 of Fig. 3),
    - microprocessor, (indirectly through 216 of Fig. 3) and
    - data compression/decompression module (212 of Fig. 3).

33. **With respect to claim 6**, Pattisam et al. disclose

- the storage device capable of increasing transmission speed as in claim 2 (see above paragraph 29),
- wherein said data compression/decompression module (222 of Fig. 3) is
    - embedded in said controller (20 of Fig. 3) and
    - between said system interface (205 and 206 of Fig. 3) and said memory interface (215 of Fig. 3).

Claim Rejections - 35 USC § 103

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. **Claims 7-9 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pattisam et al. (US 5,357,614.

36. **With respect to claim 7**, Pattisam et al. disclose a storage device capable of increasing transmission speed, mainly comprising

- a controller (20 of Fig. 3) and
- at least a solid-state storage medium (240 of Fig. 3);
- said controller has
    - an internal system interface that may be connected to an external system end (communications lines 205 and 206 of Fig. 3),
    - a microprocessor that processes system instructions (230 of Fig. 3), and
    - a memory interface that communicates with said solid-state storage medium (215 of Fig. 3);
- wherein said storage device is featured with:
    - a data compression/ decompression module (222 of Fig. 3; decompression function detailed in column 17, lines 26-31) is devised between said system interface and said memory interface and
    - is used to compress the raw data transferred via said system interface into compressed data (column 12, lines 33-35) to increase the data transmission speed in said storage device (inherent effect of a compression controller);
- a front-end data cache area comprising multi-tiered system-end data caches (210 and 211 of Fig. 3) is devised between said data compression module and said system interface and is designed into a multi-tiered structure;

- wherein every tier of system-end data cache and its next tier of system-end data cache receive and transfer data alternatively in parallel to implement parallel raw data transmission between said data compression/decompression module and said system interface (column 11, lines 65-69 – column 12, lines 1-17);

- a rear-end data cache area comprising multi-tiered memory data caches is devised between said data compression module and said memory interface and is designed into a multi-tiered structure (250 of Fig. 3).

Pattisam et al. do not disclose explicitly the rear-end data cache area wherein every tier of memory data cache and its next tier of memory data cache receive and transfer data alternatively in parallel to implement parallel compression data transmission between said data compression/decompression module and said memory interface.

However, Pattisam et al. disclose parallel compression data transmission for the front-end cache area (column 11, lines 65-69 – column 12, lines 1-17).

At the time of the invention, it would have been obvious to a person ordinary skill in the art to apply the parallel transmission of the front-end buffers to the rear-end buffers. The motivation for doing so would have been because "double buffers provide the flexibility needed to accommodate the different data rates into and out of the buffers while maintaining an overall high throughput by minimizing any wait time that may be incurred while waiting to transfer data" (column 12, lines 22-26) from the compression module to the solid-state memory.

Therefore, it would have been obvious to modify Pattisam et al. in view of their own teachings for the benefit of a data compression controller with both front-end and rear-end double buffers to obtain the invention as specified in claim 7.

37. **With respect to claim 8**, Pattisam et al. disclose the storage device capable of increasing transmission speed as in claim 7 (see above paragraph 36), wherein

- said data compression/decompression module has a decompression mechanism (222 of Fig. 3), which is triggered by the microprocessor to decompress the compressed data in the solid-state storage medium into original raw data and transfer the raw data to the external system end (column 17, lines 26-31).

38. **With respect to claim 9**, Pattisam et al. disclose the storage device capable of increasing transmission speed as in claim 7 (see above paragraph 36), wherein

- said data compression/decompression module is embedded in said controller (222 of Fig. 3 is embedded in 20 of Fig. 3).

39. **With respect to claim 12**, Pattisam et al. disclose the storage device capable of increasing transmission speed as in claim 8 (see paragraph 37 above), wherein

- said data compression/decompression module is embedded in said controller (222 of Fig. 2 is embedded in 20 of Fig. 3).

40. **Claims 10 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pattisam et al (US 5,357,614) as applied to claim 7 above in paragraph 36 and further in view of Chung (US 6,937,276).

41. **With respect to claim 10**, Pattisam et al. disclose

- the storage device capable of increasing transmission speed as in claim 7 (see above paragraph 36).

Pattisam et al. do not disclose the storage device of claim 7 wherein the storage capacity of said rear-end data caches is equal to that of the front-end data caches.

Chung discloses a compression device wherein

- the storage capacity of a rear-end data cache (71 of Fig. 4)
- is equal to that at the front-end data cache (73 of Fig. 4) (column 5, lines 26-38 describe how "The compression algorithm will typically afford compression ratios of 50%, so that two megabytes of initial image information 67i generates but one megabyte of secondary image information... This secondary image information 67s is then stored in a frame buffer 73...For this example, then, the frame buffer should be at least one megabyte in size," which includes a buffer of two megabytes and, therefore, a rear-end cache with storage capacity equal to that of the front-end cache).

Pattisam et al. and Chung are analogous art because they are from the same field of endeavor, namely data compression and storage.

At the time of invention it would have been obvious to a person of ordinary skill in the art to combine Chung's rear-end buffer with a storage capacity equal to that of the front-end buffer with the data compression controller with parallel front-end and rear-end buffers of Pattisam et al. According to Chung, the motivation for doing so would have been because "the frame buffer 73 must have a memory size of at least r bits, [where r bits is the size of the secondary, compressed image data; column 5, lines 24-25] and

ideally a size that is at least slightly larger than r bits to accommodate for any variations in the compression ratios of the initial image information"(column 5, lines 33-36). If the data cannot be compressed, a rear-end buffer equal in storage capacity to the front-end buffer is needed to hold all of the data.

Therefore, it would have been obvious to combine Chung with Pattisam et al. for the benefit of a data compression controller with rear-end caches with a storage capacity equal to that of the front-end caches.

42. **With respect to claim 11**, Pattisam et al. disclose

- the storage device capable of increasing transmission speed as in claim 7 (see above paragraph 36).

Pattisam et al. do not disclose the storage device of claim 7 wherein the storage capacity of said rear-end data caches may be smaller than that of the front-end data caches according to the compression ratio.

Chung discloses

- a compression device wherein the storage capacity of a rear-end data cache (71 of Fig. 4) is smaller than that at the front-end data cache (73 of Fig. 4) according to the compression ratio (column 5, lines 26-38 describe how "The compression algorithm will typically afford compression ratios of 50%, so that two megabytes of initial image information 67i generates but one megabyte of secondary image information... This secondary image information 67s is then stored in a frame buffer 73...For this example, then, the frame buffer should be at least one megabyte in size").

Pattisam et al. and Chung are analogous art because they are from the same field of endeavor, namely data compression and storage.

At the time of invention it would have been obvious to a person of ordinary skill in the art to combine Chung's rear-end buffer with a storage capacity equal to that of the front-end buffer with the data compression controller of Pattisam et al. The motivation for doing so would have been because "the memory requirements of the frame buffer can thus be correspondingly reduced, which leads to less expensive component costs" (column 3, lines 41-44).

Therefore, it would have been obvious to combine Chung with Pattisam et al. for the benefit of a data compression controller with rear-end caches with a storage capacity smaller than that of the front-end caches according to the compression ratio.

Conclusion

43. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US 6,847,315 teaches a compressed main memory with multiple caches for the compression controller;
- US 6,446,145 teaches a compression controller with a single cache exclusively for writing to main memory between the system interface and the compression/decompression module;
- US 6,145,069 teaches a compression controller with a single cache between the system interface and compression/decompression module;

- US 2004/0015660 teaches a compression controller with a single cache between a network interface and compression/decompression module.

44. Per the instant office action, claims 1-12 have received a first action on the merits and are the subject of a first action non-final.

45. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James R. Golden whose telephone number is 571-272-5628. The examiner can normally be reached on Monday-Friday, 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, Donald Sparks, the examiner's supervisor, can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James R. Golden
Assistant Examiner
Art Unit 2187

DONALD SPARKS
SUPERVISORY PATENT EXAMINER

September 22, 2005